Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 10. A fabrication method for a flash memory device, comprising:
providing a first conductive type substrate, wherein the substrate comprises a second conductive type first well region, a first conductive type second well region and a stacked gate structure which are sequentially formed thereon;
forming a source region and a drain region in the substrate beside two sides of the stacked gate structure;
forming a spacer on a sidewll of the stacked gate structure;
forming a first patterned photoresist layer on the substrate, the first patterned photoresist layer exposes the substrate at the drain region;
etching the substrate at the drain region until penetrating through the junction between the drain region and the first conductive type second well region by using the first patterned photoresist layer and the stacked gate structure with the spacer as a mask;
removing the first patterned photoresist layer;
forming a second patterned photoresist layer on the substrate, the second patterned photoresist layer ex-

poses the substrate at the source region;

etching the substrate at the source region to the second conductive type first well region to form a trench by using the second patterned photoresist layer and the stacked gate structure with the spacer as a mask;

performing an ion implantation process to implant dopants at a bottom and a sidewll of the trench on the substrate to form a doped region;

removing the second patterned photoresist layer;

forming a first conductive layer on the substrate, wherein the first conductive layer fills a gap between the stacked gate structure;

removing a portion of the first conductive layer to form a first contact on the source region and a second conductive layer on the first conductive type second well region, wherein the first contact electrically connects with the source region and the doped region;

patterning the second conductive layer to form a second contact, wherein the drain region and the first conductive type second well region are short-circuited by the second contact;

forming an interlayer dielectric layer on the substrate; and

forming a conductive line on the interlayer dielectric layer, wherein the conductive line electrically connects with the second contact.

[c2] 11. The method of claim 10, wherein the ion implantation process includes a tilt angle ion implantation process.

[c3] 12. The method of claim 11, wherein a tilt angle for the ion implantation process is about 15 degrees to about 30 degrees.

[c4] 13. The method of claim 10, wherein the bottom of the trench and the sidewall of the trench form an obtuse angle.

[c5] 14. The method of claim 10, wherein the dopants of the ion implantation process, the source region and the drain region are the same.

[c6] 15. The method of claim 10, the method further comprising a step of forming a plug in the interlayer dielectric layer, wherein the plug electrically connects the conductive line and the second contact.

[c7] 16. The method of claim 10, wherein the first conductive type substrate includes a P-type substrate.

[c8] 17. The method of claim 10, wherein the second conductive type first well region includes an N-type well region.

[c9] 18. The method of claim 10, wherein the first conductive type second well region includes a P-type well region.

[c10] 19. The method of claim 10, wherein the step of removing the first conductive layer includes performing back etching.

[c11] 20. The method of claim 10, wherein the step of removing the first conductive layer includes performing chemical mechanical polishing